REMARKS

The preliminary amendment filed September 15, 2003 added claims 72-86 as claims 72-82 and 84-87 because claim 83 was inadvertently skipped when the claims were numbered. In this amendment, each claims is referred to by its correct claim numbering.

Claims 72, 76, 78, 81-82, and 84 have been amended. Claims 75 and 85-86 has been canceled. No new claims have been added. Claims 72-74 and 76-84 are pending.

Claims 78 and 83-86 stand objected to due to minor informalities. Claims 78, and 82-85 have been amended as suggested in the Office Action. Claim 86 has been canceled. Accordingly, the objection to claims 78 and 83-86 should be withdrawn.

Claims 72-76 and 81-85 stand rejected under the judicially created doctrine of non-statutory double patenting in view of claim 1 of U.S. Patent No. 6,647,470. A Terminal Disclaimer with respect to U.S. Patent 6,647,470 is being concurrently filed with this response. Accordingly, the double patenting rejection to claims 72-76 and 81-85 should be withdrawn.

Claims 72-85 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Shepherd (U.S. Patent No. 6,434,665). This rejection is respectfully traversed.

Claims 72 recites, *inter alia*, "when said control signal is in a first state the memory device is caused to perform a write operation while posting said input data by storing said input data in a temporary storage area, transferring said input data from said temporary storage area to a write latch, and writing said input data from said write latch to an array of said memory device when said array is available for access."

Claim 76 recites, *inter alia*, "wherein said memory device includes a write latch and a buffer for storing said input data when said input data is posted, and said input data is transferred to a write latch and subsequently written to an array of said memory device when said array is available for writing."

Claims 81 and 84 recite, *inter alia*, "transferring said input data to a write latch associated with said array; and writing said input data from said write latch to said array when said array is available for writing."

Shepherd discloses a cache memory system which can reorder a sequence of read and write transaction to increase the throughput of the cache memory system. Reads and writes can be advantageously reordered to increase throughput because writes require more time to process than reads in a cache memory. Accordingly, rescheduling a sequence of read and write transaction can be performed to avoid stalling a read transaction which immediately follows a write transaction.

Each of the independent claims recite the use of a write latch which is used when write data is ultimately written to an array of a memory device. This feature is not taught or suggested by Shepherd. Although Shepherd discloses in Fig. 2 a store buffer 220 for supporting posted writes by accepting write data, that write data is directly written from the store buffer 220 to the array of the memory. Accordingly, Shepherd fails to teach or suggest the use of a write latch for writing an array of a memory when the array is available for writing.

Claims 72, 76, 81, and 84 are believed to be allowable over the prior art of record. Depending claims 73-74, 77-80, and 82-83 are believed to be allowable for at least the same reason as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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